REMARKS

The claims are claims 1 to 14, 33 and 34.

Claims 1 and 33 are amended. Claims 26 to 32 are newly cancelled. Claims 1 and 33 are amended in response to the rejection under 35 U.S.C. 112.

Claims 1 to 14 and 33 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The OFFICE ACTION states that the recited successive transistor paths recited in claims 1 and 33 is not corresponding to any element disclosed in the specification and drawings.

Claims 1 and 33 have been amended to correct the recitation of the successive transistor paths. Claims 1 and 33 now recite the successive transistor paths traverse the first compressor from an input to a carry output, between the first and second compressors, and traverse the second compressor from input to the summation output. This recitation corresponds to the definition recited in paragraphs [0008] and [0009] of the application. Such successive transistor paths are described in: paragraph [0008] and denoted path (C) and (D) illustrated in Figure 2; paragraph [0012] and denoted path (F) illustrated in Figure 3; and paragraph [0015] and denoted path (H) illustrated in Figure 4. The Applicants respectfully submit that claims 1 and 33 now recite subject matter described in the application.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

Robert D. Marshall, Jr.
Reg. No. 28,527